3,855,6109, Masuda).

Applicants gratefully acknowledge the indication that Claims 6-16 and 19 would be allowed if rewritten to be in independent form so that Claim 6 would include all of the limitations of Claims 5, 3, and 1; Claim 9 would include al of the limitations of Claims 5, 3, and 1; Claim 11 would include al of the limitations of Claims 5, 3, and 1; Claim 12 would include al of the limitations of Claims 5, 3, and 1; Claim 16 would include al of the limitations of Claims 5, 3, and 1; and Claim 19 would include al of the limitations of Claims 18, 4, and 2. However, as ultimate base Claims 1 and 2 are clearly allowable over the references applied, the rejection of base Claims 1 and 2 is traversed below.

The outstanding Action first adopts the reasoning for the rejection presented in the Office Action mailed on December 20, 2000, hereinafter referred to as the December 20 Action. It then suggests that Blake, Gunning, and Masuda are relied upon as sources of definitions and teachings alleged to be "well-known to one having ordinary skill in the art." The evidence offered to support the assertion of these teachings being "well-known" is not the proper kind of evidence under the well established rule of In re Ahlert, 165 USPQ 418, 421 (CCPA 1970) requiring that "assertions of technical facts in areas of esoteric technology must always be supported by citation of some reference work." Patents, even plural patents, have been held to not be weighty evidence of wide spread recognition. See In re Barr, 170 USPQ 330, 333-34 (CCPA 1971) ("[W]e agree with the solicitor that these patents are not weighty evidence of art recognition . . . .") .

In any event, even if the teachings of Blake, Gunning, and Masuda are considered along with those of Iwamatsu, Agari, and Chen, the result of that consideration is not the subject matter of Claims 1-5 and 18.

Turning to the reasoning for the rejection presented in the December 20 Action, the

reliance stated at page 2 thereof as to Chen is with regard to col. 7, lines 29-34 which is misstated to teach the doping of "the body of an SOI MOS transistor [to] minimize the RC time constant due to the body link." What col. 7, lines 29-34 actually teach is controlling the RC time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" by providing an "appropriate doping concentration in recessed region 20." No doping of the body of any SOI MOS transistor is taught "[to] minimize the RC time constant due to the body link" as erroneously stated here.

Moreover, while Chen further states (at col. 3, lines 19-22) that field effect transistors 26 formed on the mesas 24 have a "body" and that these "bodies of field effect transistors 26 are in ohmic contact due to recessed region 20 of silicon layer 18," this has no relevance to doping the "body link or recessed region 20" that extends from "a respective channel" of each transistor to the "substrate contact 39."

Moreover, as Chen already defines the body of each of these field effect transistors 26 to be apart from recessed region 20 that then serves to "link" (hence the name "body link") each of these bodies of field effect transistors 26 to substrate contact 39, the reason why the artisan would look to Blake to define a transistor body is not set forth in violation of recent precedent. See In re Rouffet, 47 USPQ2d, 1453, 1459 requiring the PTO to "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." [Emphasis added.]

Furthermore, whatever Blake defines to be a "body node" (at col. 1, lines 55-58) in terms of an "undepleted volume within the body region underlying the gate electrode," in no way modifies the teachings of Chen that there is a "body link, or recessed region 20 from a respective channel to substrate contact 39" that is separate from the "bodies" of transistors 26 as Chen uses these terms. Clearly, each transistor "body" 26 of Chen is not the same thing as

the "body link" that is equated by Chen to the recessed region 20 at col. 7, line 3.

Furthermore, page 2 of the outstanding Action errs in suggesting that the word "body" can be taken out of context from the other teachings of Chen. Such an approach is prohibited by the PTO reviewing court in In re Kotzab, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) as follows:

> While the test for establishing an implicit teaching, motivation, or suggestion is what the . . . statements of [the reference] would have suggested to those of ordinary skill in the art, the [reference] statements cannot be viewed in the abstract. Rather, they must be considered in the context of the teaching of the entire reference. [Emphasis added.]

In addition, the teachings of Blake at col. 1, lines 55-68 and col. 5, lines 23, 33, 37, and 53-60, all noted as being relied upon in the outstanding Action, make it clear that the "body node," the "undepleted volume under the gate electrode, " is below the channel of transistor 100 when conducting," see Blake at col. 5, lines 59-60. This means that Blake teaches the body node is actually more distant from any gate electrode and gate electrode capacitance than immediately below the channel. See the "depletion regions" of Figs. 35 and 36 from pages 203 and 204 of Sze, SEMICONDUCTOR DEVICES, Physics and Technology, 1985, attached hereto. Just as gate capacitance between a gate and the substrate surface it is separated from by a gate oxide is not a capacitance "in the body link or recessed region 20" of Chen, it is also not a capacitance in the body node of Blake.

Clearly, those skilled in the art would have no reason to believe that the "body link" of Chen relates to the channel 32 illustrated in Fig. 1 of Chen or anything illustrated to be above that channel such as the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, see col. 3, lines 15-18 of Chen. Thus, the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added)

precludes any consideration of gate capacitance relative to the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, at least to those familiar with the clear meaning of the words used by Chen.

Thus, applicants do not argue that the prior art does not recognize the existence of gate capacitance as alleged at page 3 of the outstanding Action; instead, the argument is clear that whatever the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) might be, it cannot be **REASONABLY** said to be gate capacitance between the surface above channel 32 separated from gate 27 by gate oxide 34, as none of these elements are "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added). As noted above, just as gate capacitance between a gate and the substrate surface it is separated from by a gate oxide is not a capacitance "in the body link or recessed region 20" of Chen, it is also not a capacitance in the body node of Blake.

The argument of the Appeal Brief at pages 11-12 pointing out true sources of "C" "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) was just that, not a denial that gate capacitance does not exist **ELSEWHERE**. This argument remains relevant as the mere indication by Gunning of "drain-side capacitances," source-side capacitances" and "gate-substrate capacitance" and that of Masuda as to "C_{GP},""C_{GS}," and "C_{PS}," do not change the simple fact that the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added). Accordingly, this relevant argument is repeated as follows:

> The [final rejection] is further mistaken in ignoring the limitation of

concern in Claim 1 (and Claim 2, for that matter) requires "C" to be gate capacitance and not simply some form of stray capacitance or junction parasitic capacitance like the capacitances noted at col. 1, lines 20-22, or col. 5, lines 9-11, which is the parasitic capacitance under drain 28 and source 30 junctions of Chen. Moreover, Chen describes (in col. 3, lines 56-60) a doping concentration of the recessed region 20 and the depletion width between the source and/or drain region and the recessed region 20. This further description clearly concerns the junction capacitance between the source and/or drain region and the recessed region 20 noted as to col. 5, lines 9-11, and it is well known that a capacitance value of such a junction capacitance is highly influenced by the doping concentration of the recessed region 20.

Furthermore, the response filed March 20, 2001, noted the following:

> In addition to lacking any evidence that the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to control, the Action further lacks any evidence that the artisan would have a prior art based reason to believe that this RC product having an R value and a C value from different elements is somehow a measure of how quickly the signal decays as stated at the top of page 3 of the Action. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired result. As noted by In re Sporck, 133 USPQ 360, 364 (CCPA 1962):
>
> > Obviousness is a legal conclusion which we ware required to draw from facts appearing in the record or of which judicial notice may be taken. Thus before we can conclude that any disclosed invention is 'obvious' under the conditions specified in 35 U.S.C. §103, we must evaluate facts from which to determine (1) what was shown in the prior art at the time the invention was made, and (2) the knowledge which a person of ordinary skill in the art possessed at the time the invention was made. Here, neither the record nor the facts of which we are able to take judicial notice supplies the factual data necessary to support the legal conclusion of obviousness of the invention at

> the time it was made. We are unwilling to substitute speculation and hindsight appraisal of the prior art for such factual data.

Thus, it is clear that the examiner improperly attempts to suggest that because Chen does not explain how the "C" portion of the referenced RC time constant arises because of doping in recessed region 20, she can substitute a speculative assumption that some form of MOS transistor capacitance is really being referenced. Taking this speculative assumption one step further, gate capacitance is then, apparently, arbitrarily selected from known forms of transistor capacitance because this is what Claims 1 and 2 require and not because of any teaching or suggestion in any relied upon reference. The examiner, thus, does not reasonably attempt to supply a concrete factual basis for her rejection. Instead, she improperly substitutes speculation, unfounded assumptions, and hindsight reconstruction in clear violation of the above noted case law and the even more recent requirement for concrete evidence set forth by the PTO reviewing court in In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001) as follows:

> With respect to core factual findings in a determination of patentability, however, the Board cannot simply reach conclusions based on its own understanding or experience — or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings. [Emphasis added, foot note omitted.]

Just as the Board cannot substitute conclusions based upon its own understanding or experience for concrete evidence in the record, neither can the examiner.

Again, the evidence that is lacking is not that it is known that gate capacitance exists; rather, it is the lack of evidence that the artisan would expect gate capacitance to be present "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added).

Moreover, it appears from the actual context of Chen that the "C" recited at col. 7, lines 29-33, is the junction capacitance from the background discussion at col. 1, lines 20-22, the lessening of which is said to lead to higher circuit speed. As further noted at col. 5, lines 6-11 of Chen, when "silicon layer 18 is fully-depleted under drain '28' and source 30 junctions for eliminating the parasitic capacitance and gaining circuit speed." col. 5, lines

11-14 of Chen go on to note that such full-depletion may require "counter-doping by ion implantation . . . to make the area beneath the source and drain fully depleted." This is clearly doping providing an "appropriate doping concentration in the body link 20" that will provide further circuit speed. While col. 5, lines 19-27, of Chen go on to discuss the relationship of "sheet resistence of recessed region 20" and doping level in this recessed region 20, conspicuous by its absence is any hint of any concern with gate capacitance.

In this regard, it is the burden of the PTO to demonstrate a *prima facie* case of obviousness which means the PTO must show that the relied upon references teach all of the limitations of the claims without resort to speculation to fill gaps missing from reference teachings. Note the following from In re Warner, 154 USPQ 173, 178 (CCPA 1967):

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. To the extent the Patent Office rulings are so supported, there is no basis for resolving doubts against their correctness. Likewise, we may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual bases supporting its legal conclusion of obviousness. [Emphasis added.]

Instead of such evidence, page 3 of the outstanding Action seeks to substitute distortion of the actual teaching of col. 7, lines 29-34 of Chen as to of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) into a teaching that "refers to the total RC time constant" that is then further distorted to be the "sum of all contributing RC time constants as explained in the Agari reference."

The express teaching of Chen as to of controlling the "RC" time constant "in the body

link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) is ignored in violation of In re Kotzab, supra, and this error is compounded by a further distortion of the Agari teachings as to "minimizing RC delay from the resistance value and the capacitance value of each wiring part" (emphasis added, see the bottom of page 2 of the December 20 Action) into some kind of "sum of all contributing RC time constants" from other than just wiring parts. The basis for this distortion of the actual teachings of Agari has been omitted in clear violation of the directive in In re Rijckaert, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) ("When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference.").

Moreover, where is the discussion to be found of the In re Roufett, supra, required reasons explaining why "one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." [Emphasis added.]. Again, the express teaching of Chen is to capacitance "C" "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added), while the express Agari teachings relate to the capacitance "C" between wiring parts spaced from each other above a substrate surface.

Furthermore, Gunning is a reference concerned with "drivers and receivers for interfacing CMOS (complementary metal oxide semiconductor) digital circuits to transmission lines and, more particularly to relatively low power drivers and relatively sensitive receivers for interfacing VSLI (very large scale integrated) CMOS circuits to relatively low impedance, terminated transmission lines" as noted at col. 1, lines 6-12. Where are the Roufett reasons why one of ordinary skill in the art would have been motivated to select Gunning and Chen and to combine them or is the examiner suggesting that col. 7, lines

4-11 description of the Fig. 4 VLSI CMOS transmission line GTL driver is in actuality explaining the Chen SOI CMOS integrated circuit operation?

Once again, conjecture and assumptions are substituted for evidence in terms of unreasonably lifting unrelated reference teachings from the context of disparate references and then augmenting them in an irrational manner using the present claims as the guide. This approach was noted to be improper at pages 8 and 9 of the Appeal Brief as follows:

> Accordingly, what is clearly missing from the rejection is some reasonable basis to expand the teachings of Agari from a concern with wiring spacing capacitances and associated wiring resistance having an RC delay to be minimized into a concern with the capacitance of a gate and the resistance of a fixed potential transmission path extending from at least one body contact to a body region of Iwamatsu, where neither Agari or Iwamatsu present any reason to believe that the artisan would be concerned with wiring delay other than relative to illustrated X and Y wiring lines of Iwamatsu given the above-noted teachings of Agari clearly relate to designing a wiring mask layout for external wiring, not the layout of an MOS transistor formed on an SOI layer. In this regard, the response filed on March 20, 2001, indicated that:
>
> > The Action appears to suggest (at the top of page 3) that Agari somehow teaches minimizes the RC time constant of a body contact because of the improperly extracted reference to a "wiring part" at the bottom of page 2 of the Action. However, it is clear that Agari actually teaches the optimizing of wiring line widths and spacings in terms of minimizing the RC delay of a "wiring part," where the term "wiring" is one the artisan would not use to describe a body contact portion. Thus, when the "PURPOSE" and all of the "CONSTITUTION" portions of the "ABSTRACT" are read together to understand what Agari is referring to as a "wiring part" and the typical use of the term "wiring" is considered, it is clear that line width and spacing are relative to standard surface wiring and this width and spacing of the "wiring part" are controlled to minimize RC delay by controlling values of resistance and capacitance corresponding thereto. In this last regard, it is well established to be "impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (In re Wesslau, 147 USPQ 391, 393 (CCPA 1965)).
>
> Thus, the teachings of Agari taken in context, as they must be taken,

are clearly stated to be directed determining a wiring mask layout "so that the line and space at each wiring part may be the optimum line and space calculated respectively" (emphasis added). The [final rejection] improperly ignores that it is time delays due to wiring parts that have lines with capacitance inducing spaces there between that are the concern and improperly suggests that these clear teachings of Agari as to planning actual wiring layout with well defined spaces and corresponding capacitance effects would be interpreted as teachings to apply to something other than the similar surface wiring lines shown as x and y by Iwamatsu. Missing, however, is the "logical reason apparent from positive, concrete evidence of record" (In re Regel, 188 USPQ 136, 139 n.5 (CCPA 1975)) why the artisan would have been reasonably led to conclude that something other than planning the layout of wiring like the wiring lines shown as x and y by Iwamatsu was being suggested by Agari.

Besides this improper conjecture as to the teachings of Agari, the outstanding Action repeats the analysis of Claims 1 and 2 from the December 20 Action by incorporating it. Thus, the improper analysis of Claims 1 and 2 continues as noted in the Appeal Brief as follows:

> Turning to the outstanding final rejection of Claims 1 and 2 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Agari and Chen, it is first noted that the FR adopts the reasoning presented in the Office Action mailed on December 20, 2000, hereinafter referred to as the December 20 Action. This December 20 Action first incorrectly notes that Iwamatsu "teaches each of the structural elements of Claims 1 and 2" while ignoring that the subject matter of Claims 1 and 2 actually involves methods of designing a semiconductor device including a MOS transistor, where each of these claims require a different manner of determining a layout pattern for the MOS transistor. The layout pattern of Claim 1 must be determined based on the operating frequency of a predetermined clock that must have a frequency "f" greater than 500 MHZ while the layout pattern of Claim 2 must be determined based on a signal propagation delay time "td" required for the MOS transistor that is less than 50 ps.
>
> Claim 1 further requires the meeting of a specific conditional expression "R•C•f<1," with "f" as defined above, with R being the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between a first semiconductor region of first conductivity type and a second semiconductor region also of the first conductivity type, with the first and second semiconductor regions both being in an SOI layer of the MOS transistor, and C being the gate capacitance of the MOS transistor. Claim 2 further requires the meeting of a specific conditional expression "(R•C)/td<1," with "td," "R,"

and "C" as defined above.

While Agari may teach designing a semiconductor device in a manner minimizing RC delay from the resistance value and the capacitance value of each wiring part using a wiring layout and Chen may teach controlling doping of the body of an SOI device so that the RC time constant in the body link or recessed region 20 from a respective channel to the substrate contact 39 can be as short as or less than 1 nsec, a wiring layout is not a layout pattern of an MOS transistor and doping is not a step of providing an operating frequency of a predetermined clock, much less a step of determining a layout pattern of an MOS transistor based on the operating frequency of such a provided predetermined clock as Claim 1 recites. Thus, even if the teachings of Agari and Chen are in some reasonable manner combined with Iwamatsu, the result would not be the subject matter of Claim 1.

With further regard to Claim 2, the steps of providing a signal propagation delay time that is less than 50 ps for a MOS transistor and then determining a layout pattern of this MOS transistor based on said signal propagation delay time are also clearly not taught by Agari or Chen. Thus, even if the teachings of Agari and Chen are in some reasonable manner combined with Iwamatsu, the result would not be the subject matter of Claim 2.

Moreover, even as to semiconductor devices of Claims 3 and 4, the criticality of the layout patterns being appropriately determined cannot be dismissed in terms of the structural relationships that still must exist in the manufactured semiconductor device in terms of the above-noted parameters of "R" and "C" having values that taken with a frequency "f" having a value greater than 500 MHZ will satisfy the conditional expression "R•C•f<1" and that taken with a propagation delay time "td" having a value that is less than 50 ps will satisfy the conditional expression "(R•C)/td<1."

Proper and reasonable interpretations of claim limitations are clearly required if the PTO is to perform its well established duty of properly analyzing the differences between the claimed subject matter and the prior art. See In re Dembicziak, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) as follows:

> A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103(a) (Supp. 1998); *See Graham v. John Deere Co.*, 383 U.S. 1, 14, 148 USPQ 459, 465 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) The scope and content of the prior art; (2) the level of ordinary skill in the

> prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness. *See Graham*, 383 U.S. at 17-18, 148 USPQ at 467; *Miles Labs, Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 27 USPQ2d 1123, 1128 (Fed. Cir. 1993).

Further in this regard, note that Dembicziak indicates that "the Graham decision (148 USPQ at 467) requires "strict observance" of factual predicates to any determination of obviousness. Here, however, there has been no attempt to properly analyze the differences between the claimed invention and the prior art by giving reasonable meaning and effect to every limitation in independent Claims 1 and 2.

It is also well established that "every limitation positively recited in a claim must be given effect in order to determine what subject matter that claim defines." In re Wilder, 166 USPQ 545, 548 (CCPA 1970). Note also In re Wilson, 165 USPQ 494, 496 (CCPA 1970) ("all words in a claim must be considered in judging the patentability of that claim against the prior art").

Besides the outstanding Action and the relied upon December 20 Action failing to properly analyze the limitations of Claims 1 and 2, the relied upon December 20 Action appears to be at odds with the newly presented arguments of the outstanding Action that urge gate capacitance associated with gate 27 as being included in the capacitance"C" of concern to Chen. In this regard, page 3 of the relied upon December 20 Action states that the teaching of Agari as to minimizing "the RC time constant of each wiring part" would be applied relative to the "body contact as taught by Chen et al." However, this "body contact" language appears to be referencing substrate contact 39, not gate 27.

In essence, the outstanding Action and the December 20 Action do little more than attempt to show that there was knowledge that RC time constants associated with wiring can be controlled to control circuit speed, that the capacitance associated with the gate of an MOS transistor was also known, that the general structure of SOI MOS transistors with a single body contact was further known, and that controlling the RC time constant in a body link from below MOS transistor channels to such a single body contact was also known and

then suggest that the artisan would have been able to combine what was known to meet the claimed invention. This approach by the PTO is not new and has been routinely dismissed by the courts as improper. See the recent explanation of impropriety set forth by In re Rouffet, at 47 USPQ2d 1457-58 as follows:

> As this court has stated, "virtually all [inventions] are combinations of old elements." *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983); see also *Richdel, Inc. v. Sunspool Corp.*, 714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability." *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996).
>
> To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. [Emphasis added].

With specific regard to Claim 2 and 4, the discussion starting at the bottom of page 5 and continuing through the top of page 8 of the response filed March 20, 2001, is again believed to be relevant and is repeated here for the Examiner's convenience as follows:

> Turning to Claim 2, it is again noted that this claim is similar to Claim 1 as to the method of designing that is recited and the semiconductor device to be designed. The differences relate to the requirements of Claim 2 that relate to a signal propagation delay time being provided instead of the Claim 1 operating frequency and the determining of the layout pattern being based on this signal propagation delay time instead of the Claim 1 operating frequency. In this regard, Claim 2 requires the layout pattern to be determined so that $(R \cdot C) / td < 1$ with the definitions of R and C being the same for Claim 2 as for Claim 1 and "td" being the signal propagation delay time of the MOS transistor which must be less than or equal to 50 ps.

Once again relative to Claim 2, it is believed to be clear that if the artisan where to reasonably use the teachings of Agari and Chen to design the device of Iwamatsu, he would merely add a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by Claim 2.

Similarly, with respect to independent Claim 2, the teachings of Agari cannot be based upon extracting terms out of context and assigning meanings thereto that are not consistent with the meanings clearly used by Agari. See again the Wesslau decision discussed above. The rejection of Claim 2 is also traversed as relying upon an improper interpretation of the language "wiring part" used by Agari just as the rejection of Claim 1 was.

Moreover, and as noted above, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also taught by Chen. What Claim 2 requires, on the other hand, is the use of a layout pattern to form an MOS transistor on an SOI layer that will satisfy the conditional expression $(R \cdot C) / td > 1$ where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and td = signal propagation delay time required for the MOS transistor, with td being less than or equal to 50 ps. None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a signal propagation delay time td required for the MOS transistor, with td being less than or equal to 50 ps and insuring that the final result is less than one.

Clearly, the resistance "R" of concern in Claim 2 is again that of a "fixed potential transmission path" extending from a body contact to a body region as discussed above and not the resistance of the wiring line of concern to Agari. In addition none of Iwamatsu, Agari, or Chen teach any reason to use the capacitance "C" of the MOS transistor gate electrode along with this value R of an internal transmission path to form an RC product, much less one that meets the Claim 2 requirement that $(R \cdot C) / td < 1$ with td being less than or equal to 50 ps. Once again, valid rejections can only be made if they are based upon established facts as to the prior art. The rejection of Claim 2 is also traversed because speculation and hindsight based upon applicants' disclosure have again been used as a substitute for facts not of record.

Consequently, the rejection of Claims 2 and 4 sare traversed for the reasons noted above.

It is further noted that Claims 5 and 18 are specific to a semiconductor device having a particular resistance for the fixed potential transmission path primarily determined by body region 14 resistance defined in part by the thickness of the SOI layer times the length of the fixed potential transmission path along the gate length of the gate electrode. The various Office Actions presented throughout the present extensive prosecution have not set forth any attempt at a *prima facie* case of obviousness that addresses these limitations. Without such a *prima facie* case of obviousness, In re Fine, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988) indicates that the Claims 5 and 18 cannot be reasonably rejected under 35U.S.C. §103 and this rejection is also traversed.

As no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance. Consequently, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

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